



# 1/4-Inch System-On-A-Chip (SOC) VGA NTSC/PAL CMOS Digital Image Sensor

## MT9V135C12STC (Pb-Free CLCC)

### Features

- Micron<sup>®</sup> DigitalClarity<sup>®</sup> CMOS imaging technology
- System-On-a-Chip (SOC)—Completely integrated camera system
- NTSC/PAL (true two field) analog composite video output
- ITU-R BT.656 parallel output (8-bit, interlaced)
- Simultaneous composite and digital video outputs (simplifies focus and setup of network cameras)
- Serial LVDS data output
- Low power, interlaced scan CMOS image sensor
- Supports use of external devices for addition of custom overlay graphics
- Superior low-light performance
- On-chip image flow processor (IFP) performs sophisticated processing
- Color recovery and correction, sharpening, gamma, lens shading correction, and on-the-fly defect correction
- Automatic features:
  - Auto exposure
  - Auto white balance (AWB)
  - Auto black reference (ABR)
  - Auto flicker avoidance
  - Auto color saturation
  - Auto defect identification and correction
- Simple two-wire serial programming interface

### Applications

- Security cameras
- 900 MHz and 2.4 GHz wireless cameras
- Composite video and digital video cameras
- CCTV security cameras
- Smart cameras
- Evidence quality cameras
- Cameras using active or passive overlay

**Table 1: Key Performance Parameters**

Parameter		Typical Value
Optical format		1/4-inch (4:3)
Active imager size		3.63mm(H) x 2.78mm(V) 4.57mm diagonal
Active pixels		640H x 480V
NTSC output		720H x 486V
PAL output		720H x 576V
Pixel size		5.6µm x 5.6µm
Color filter array		RGB Paired Bayer pattern
Shutter type		Electronic rolling shutter (ERS)
Maximum data rate master clock		13.5 Mp/s 27 MHz
Frame rate (VGA 640H x 480V)		30 fps at 27 MHz (NTSC) 25 fps at 27 MHz (PAL)
Integration time (composite video output)		16µs–33ms (NTSC) 16µs–40ms (PAL)
ADC resolution		10-bit, on-chip
Responsivity		5 V/lux-sec (550nm)
Pixel dynamic range		70dB
SNR <sub>MAX</sub>		39dB
Supply voltage	I/O digital	2.5–3.1V (2.8V nominal)
	Core digital	2.5–3.1V (2.8V nominal)
	Analog	2.5–3.1V (2.8V nominal)
Power consumption		320 mW @ 2.8V, 25°C
Operating temperature <sup>1</sup>		–30°C to +70°C
Packaging		48-pin CLCC

Note: 1. Customers requiring a similar part with greater temperature range should consider using the Micron MT9V125.

**Table 2: Ordering Information**

Part Number	Description
MT9V135C12STC ES	48-pin CLCC ES, Pb-Free
MT9V135C12STCD	Demo kit
MT9V135C12STCH	Demo kit headboard



## General Description

The MT9V135 is a VGA CMOS image sensor featuring Micron's breakthrough Digital-Clarity technology—a low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, low power, and integration advantages of CMOS.

The MT9V135 performs sophisticated processing functions including color recovery, color correction, sharpening, programmable gamma correction, auto black reference clamping, auto exposure, automatic 50Hz/60Hz flicker avoidance, lens shading correction, auto white balance (AWB), and on-the-fly defect identification and correction.

The MT9V135 outputs interlaced-scan images at 30 or 25 fps, supporting both NTSC and PAL video formats.

The MT9V135 includes digital video output that can be switched to the NTSC/PAL encoder. This can be used in conjunction with an external DSP to provide an overlay (such as a logo or a menu screen) on top of the live video.

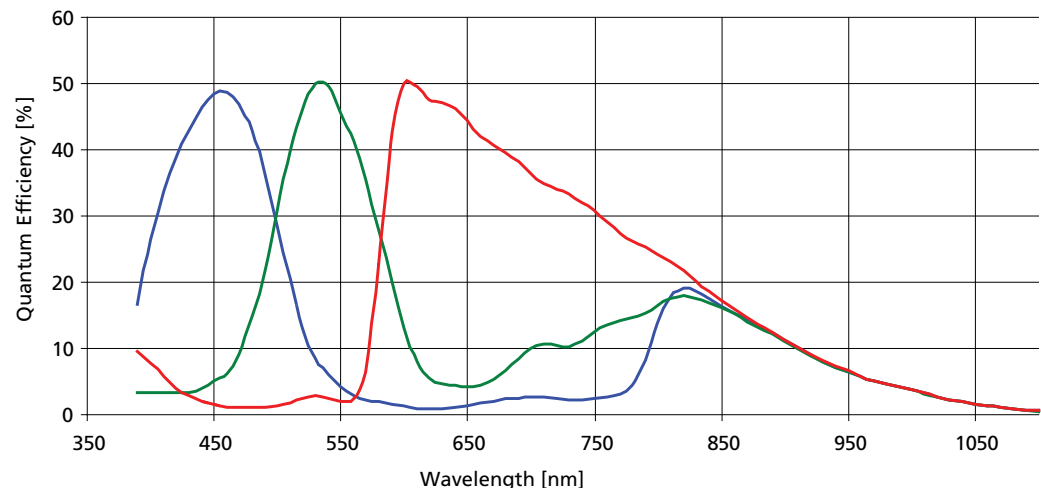
The image data can be output on any one of three output ports:

- Composite analog video (support for both single-ended and differential)
- Low-voltage differential signalling (LVDS)
- CCIR 656 interlaced digital video in parallel 8-bit format

**Table 3: MT9V135 Detailed Performance Parameters**

Parameter	Value
Output Gain	28 e-/LSB
Read Noise	5.3 e-RMS at 16X
Dark Current	1600 e-/pix/s at 70°C

**Figure 1: MT9V135 Quantum Efficiency vs. Wavelength**





## MT9V135: SOC VGA Digital Image Sensor Functional Overview

### Functional Overview

The MT9V135 is a fully-automatic, single-chip camera, requiring only a single power supply, lens, and clock source for basic operation. Output video is streamed via the chosen output port. The MT9V135 internal registers are configured using a two-wire serial interface.

The device can be put into a low-power sleep mode by asserting STANDBY and shutting down the clock. Output signals can be tri-stated. Both tri-stating output signals and entry into standby mode can be achieved via two-wire serial interface register writes.

The MT9V135 requires an input clock of 27 MHz to support correct NTSC or PAL timing.

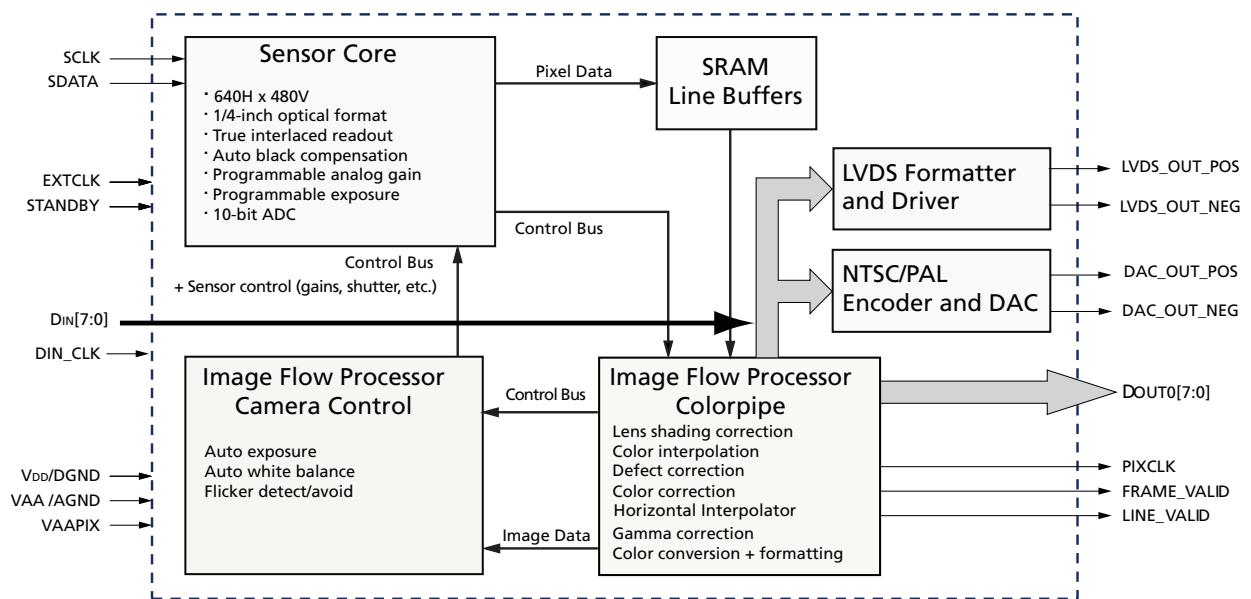
### Internal Architecture

Internally, the MT9V135 consists of a sensor core and an image flow processor (IFP). The IFP is divided in two sections: the colorpipe, and the camera controller. The sensor core captures raw images that are then input into the IFP. The colorpipe section processes the incoming stream to create interpolated, color-corrected output, and the camera controller section controls the sensor core to maintain the desired exposure and color balance.

The IFP scales the image and an integrated video encoder generates either NTSC or PAL analog composite output. The MT9V135 supports three different output ports; analog composite video out, LVDS serial out and CCIR 656 interlaced digital video in parallel 8-bit format.

Figure 2 shows the major functional blocks of the MT9V135. The built-in NTSC/PAL encoder and the LVDS Formatter allow simultaneous outputs of composite and digital video signals. This is especially useful during installation of network cameras and allows the installer to adjust the camera view and focus using analog monitoring equipment while the digital video is compressed and formatted for IP network delivery.

**Figure 2: Functional Block Diagram**

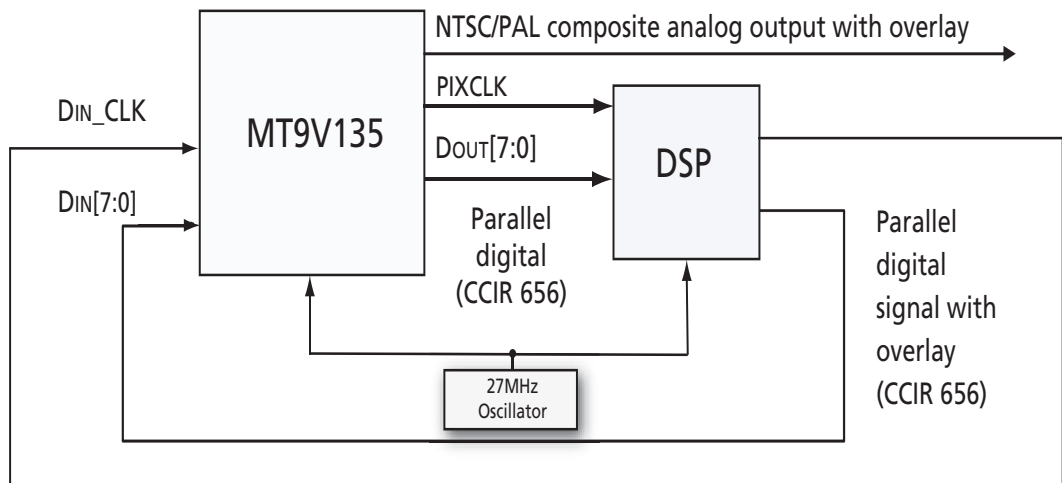




## MT9V135: SOC VGA Digital Image Sensor Functional Overview

Figure 3 shows a typical application using a DSP to produce a video overlay (such as a logo or menu text). The parallel digital video output is sent to the DSP, which adds the overlay. The digital video with the overlay is then looped back into the MT9V135 to the NTSC/PAL encoder and LVDS formatter to provide simultaneous composite analog and digital LVDS outputs.

**Figure 3: Typical Usage Configuration with Overlay**





## MT9V135: SOC VGA Digital Image Sensor Typical Connections

### Typical Connections

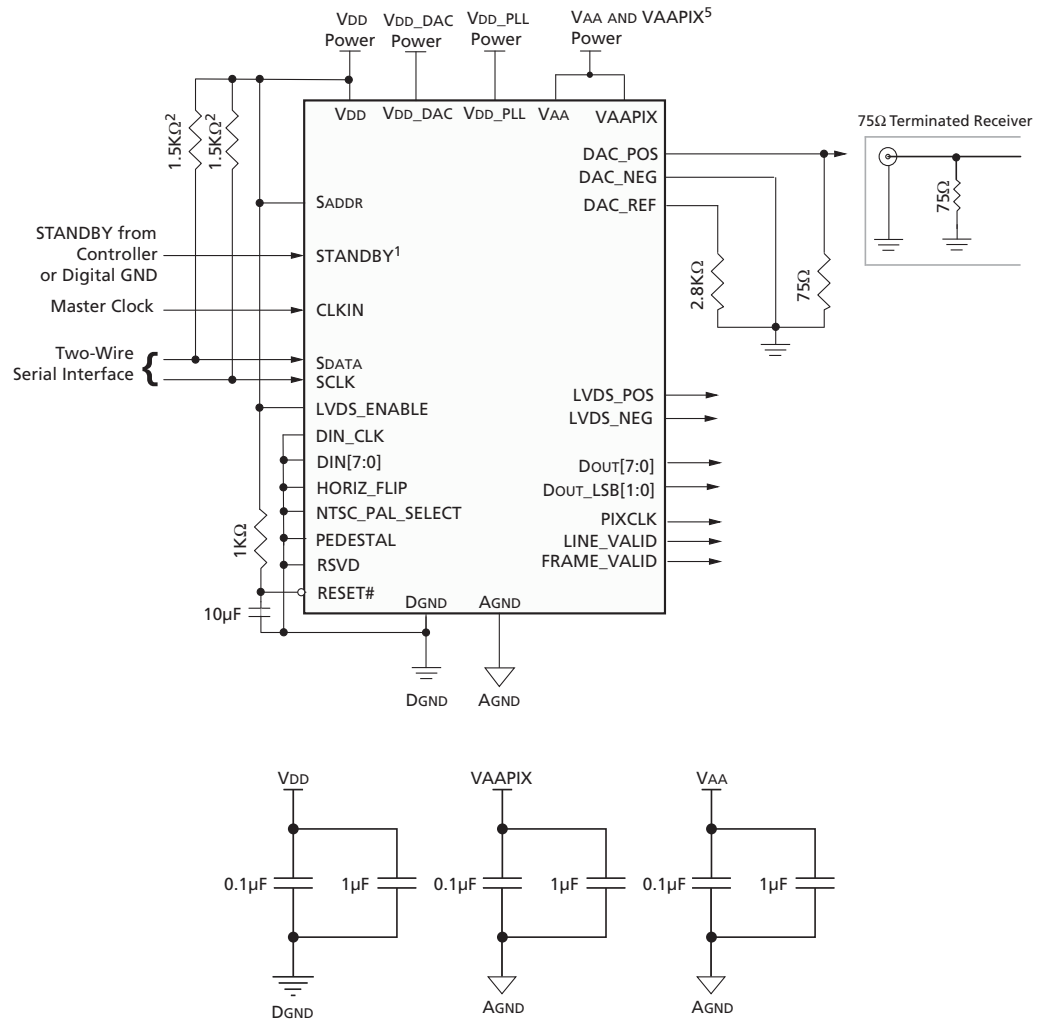
Figure 4 shows a detailed MT9V135 device configuration. For low-noise operation, the MT9V135 requires separate analog and digital power supplies. Incoming digital and analog ground conductors can be tied together next to the die.

Power supply voltages VAA (the primary analog voltage) and VAAPIX (the main voltage to the pixel array) must be tied together to avoid current loss.

Both power supply rails should be decoupled from ground using capacitors.

The MT9V135 requires a single external voltage supply level.

**Figure 4: Typical Configuration (without use of overlay)**

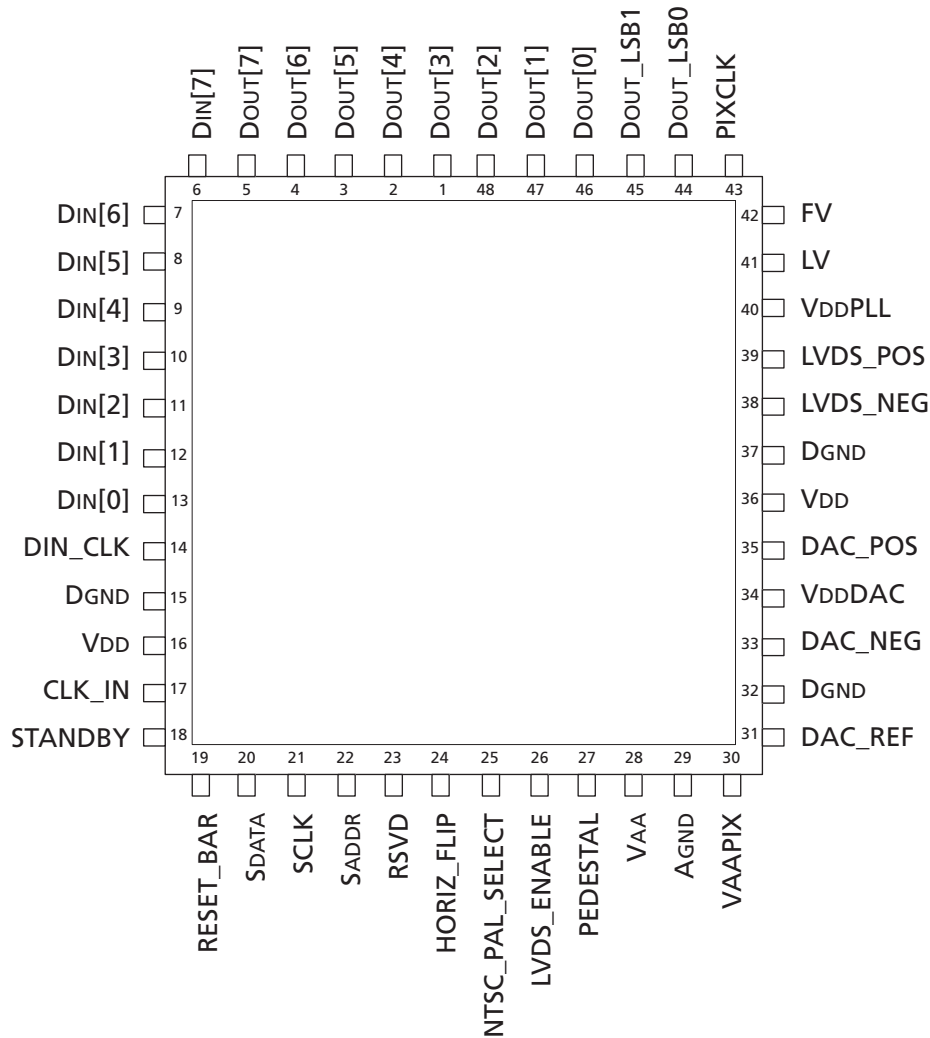


- Notes:
1. MT9V135 STANDBY can be connected to customer's ASIC controller directly or to Digital GND, depending on the controller's capability.
  2. A 1.5KΩ resistor value is recommended, but may be greater for slower (for example, 100Kb) two-wire speed.
  3. LVDS\_ENABLE should be tied HIGH if LVDS is to be used.
  4. Pull down DAC\_REF with a 2.8K ohm resistor for 1.0V peak-to-peak video output. For a 1.4V peak-to-peak video output, change the video resistor to 2.4K ohms.
  5. VAA and VAAPIX must be tied to the same potential for proper operation.



## MT9V135: SOC VGA Digital Image Sensor Typical Connections

**Figure 5: 48-pin CLCC Assignment**



**Table 4: Pin Descriptions**

Pin Assignment	Name	Type	Description
17	EXTCLK	Input	Master clock in sensor.
19	RESET_BAR	Input	Active LOW: asynchronous reset.
22	SADDR	Input	Two-wire serial interface device ID selection 1:0xBA, 0:0x90.
23	RSVD	Input	Must be attached to DGND.
21	SCLK	Input	Two-wire serial interface clock.
18	STANDBY	Input	Multifunctional signal to control device addressing, power-down, and state functions (covering output enable function).
24	HORIZ_FLIP	Input	If "0" at reset: Default horizontal setting. If "1" at reset: Flips the image readout format in the horizontal direction.
25	NTSC_PAL_SELECT	Input	If "0" at reset: Default NTSC mode. If "1" at reset: Default PAL mode.



## MT9V135: SOC VGA Digital Image Sensor Typical Connections

**Table 4: Pin Descriptions (continued)**

Pin Assignment	Name	Type	Description
27	PEDESTAL	Input	If "0" at reset: Does not add pedestal to composite video output. If "1" at reset: Adds pedestal to composite video output. Valid for NTSC only, pull low for PAL operation.
26	LVDS_ENABLE	Input	Active HIGH: Enables the LVDS output port. Must be HIGH if LVDS is to be used.
6, 7, 8, 9, 10, 11, 12, 13	DIN[7:0]	Input	External data input port selectable at video encoder input.
14	DIN_CLK	Input	DIN capture clock. (This clock must be synchronous to CLK_IN.)
20	S <sub>DATA</sub>	Output	Two-wire serial interface data I/O.
5, 4, 3, 2, 1, 48, 47, 46	DOUT[7:0]	Output	Pixel data output DOUT7 (most significant bit (MSB)), DOUT0 (least significant bit (LSB)). Data output [9:2] in sensor stand-alone mode.
44	DOUT_LSB0	Output	Sensor stand-alone mode output 0—typically left unconnected for normal SOC operation.
45	DOUT_LSB1	Output	Sensor stand-alone mode output 1—typically left unconnected for normal SOC operation.
42	FRAME_VALID	Output	Active HIGH: FRAME_VALID; indicates active frame.
41	LINE_VALID	Output	Active HIGH: LINE_VALID, DATA_VALID; indicates active pixel.
43	PIXCLK	Output	Pixel clock output.
35	DAC_POS	Output	Positive video DAC output in differential mode. Video DAC output in single-ended mode.
33	DAC_NEG	Output	Negative video DAC output in differential mode.
31	DAC_REF	Output	External reference resistor for video DAC.
39	LVDS_POS	Output	LVDS positive output.
38	LVDS_NEG	Output	LVDS negative output.
29	AGND	Supply	Analog ground.
15, 32, 37	DGND	Supply	Digital ground.
28	VAA	Supply	Analog power: 2.5V–3.1V (2.8V nominal).
30	VAAPIX	Supply	Pixel array analog power supply: 2.5V–3.1V (2.8V nominal).
16, 36	VDD	Supply	Digital power: 2.5V–3.1V (2.8V nominal).
34	VDDDAC	Supply	DAC power: 2.5V–3.1V (2.8V nominal).
40	VDDPLL	Supply	LVDS PLL power: 2.5V–3.1V (2.8V nominal).

- Notes:
1. ALL power pins (VDD/VDDDAC/VDDPLL/VAA/VAAPIX) must be connected to 2.8V (nominal). Power pins cannot be floated.
  2. ALL ground pins (AGND/DGND) must be connected to ground. Ground pins cannot be floated.
  3. Inputs are not tolerant to signal voltages above 3.1V.
  4. All unused inputs must be tied to GND or VDD.
  5. VAA and VAAPIX must be tied to the same potential for proper operation.

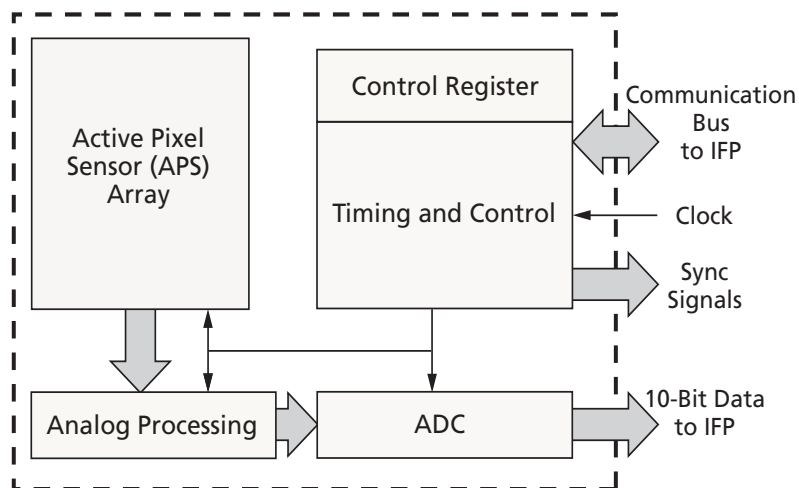


## Detailed Architecture Overview

### Sensor Core

The sensor consists of a pixel array of 695 x 512, an analog readout chain, 10-bit ADC with programmable gain and black offset, and timing and control, as illustrated in Figure 6.

**Figure 6: Sensor Core Block Diagram**

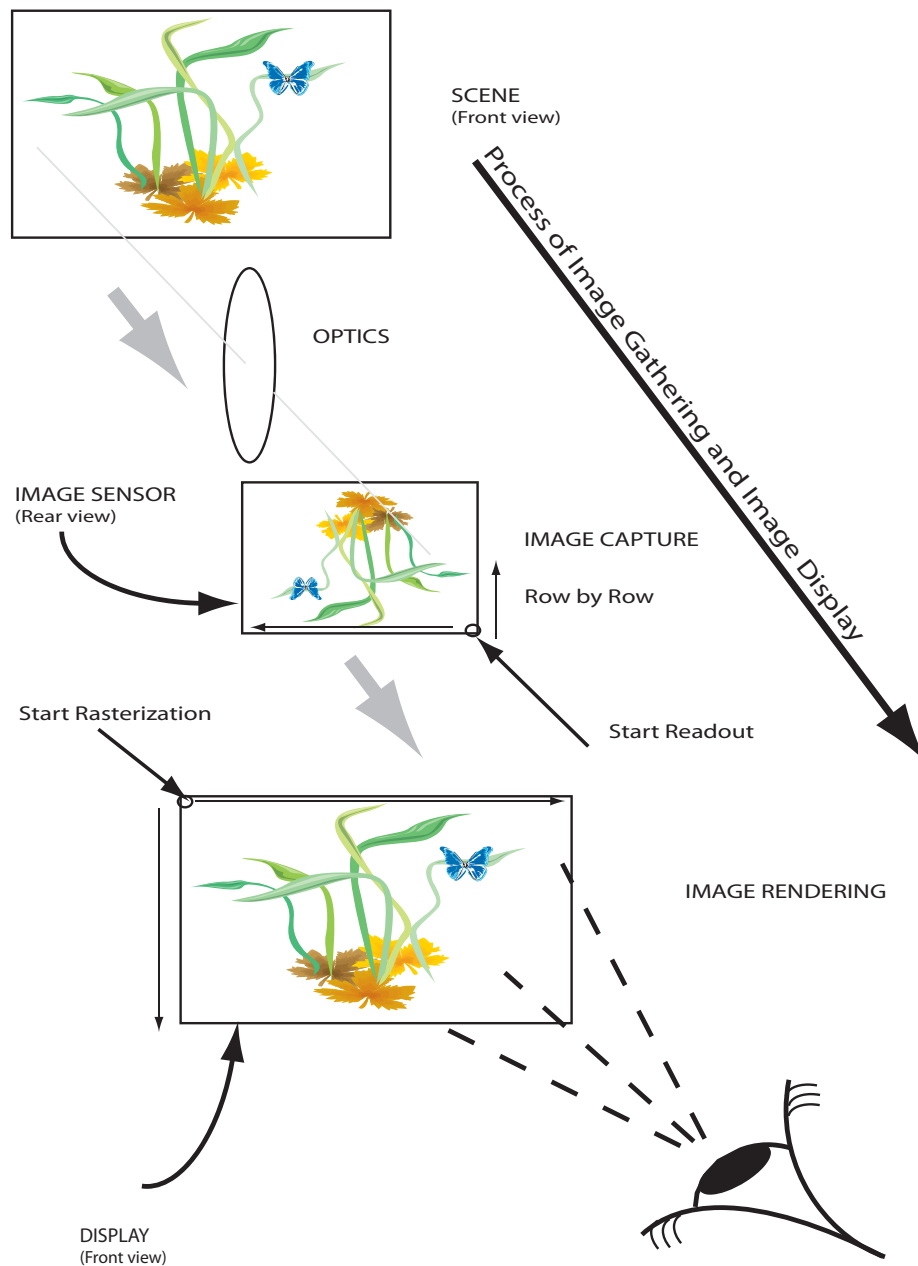


There are 649 columns by 498 rows of optically-active pixels that include a pixel boundary around the VGA (640 x 480) image to avoid boundary effects during color interpolation and correction.

The one additional active column and two additional active rows are used to enable horizontally and vertically mirrored readout to start on the same color pixel.

Figure 7 on page 9 illustrates the process of capturing the image. The original scene is flipped and mirrored by the sensor optics. Sensor readout starts at the lower right hand corner. The image is presented in true orientation by the output display.



**Figure 7: Image Capture Example**


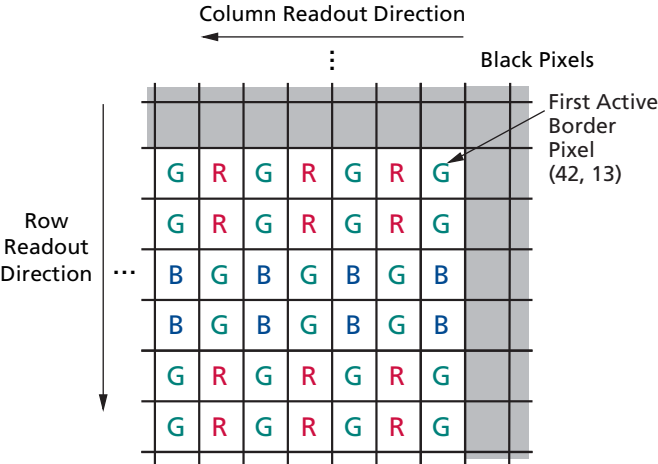
The sensor core uses a paired RGB Bayer color pattern, as shown in Figure 9 on page 11.

Row pairs consist of the following: rows 0, 1, rows 2, 3, rows 4, 5, and so on. The even-numbered row pairs (0/1, 4/5, and so on) in the active array contain green and red pixels. The odd-numbered row pairs (2/3, 6/7, and so on) contain blue and green pixels. The odd-numbered columns contain green and blue pixels; even-numbered columns contain red and green pixels.



**MT9V135: SOC VGA Digital Image Sensor  
Detailed Architecture Overview**

**Figure 8: Pixel Color Pattern Detail (top right corner)**



**Output Data Format**

The sensor core image data is read out in an interlaced scan order. Progressive readout—which is not supported by the color pipe—is an option, but is intended only for raw data output. Valid image data is surrounded by horizontal and vertical blanking, shown in Figure 9 on page 11.

For NTSC output, the horizontal size is stretched from 640 to 720 pixels. The vertical size is 243 pixels per field; 240 image pixels and 3 dark pixels that are located at the bottom of the image field.

For PAL output, the horizontal size is also stretched from 640 to 720 pixels. The vertical size is 288 pixels per field; 240 image pixels with 24 dark pixels at the top of the image and 24 dark pixels at the bottom of the image field.



# MT9V135: SOC VGA Digital Image Sensor Detailed Architecture Overview

**Figure 9: Spatial Illustration of Image Readout**

$P_{0,0} P_{0,1} P_{0,2} \dots P_{0,n-1} P_{0,n}$ $P_{2,0} P_{2,1} P_{2,2} \dots P_{2,n-1} P_{2,n}$	$00\ 00\ 00 \dots 00\ 00\ 00$ $00\ 00\ 00 \dots 00\ 00\ 00$
VALID IMAGE ODD FIELD	HORIZONTAL BLANKING
$P_{m-2,0} P_{m-2,1} \dots P_{m-2,n-1} P_{m-2,n}$ $P_{m,0} P_{m,1} \dots P_{m,n-1} P_{m,n}$	$00\ 00\ 00 \dots 00\ 00\ 00$ $00\ 00\ 00 \dots 00\ 00\ 00$
VERTICAL EVEN BLANKING	VERTICAL/HORIZONTAL BLANKING
$00\ 00\ 00 \dots 00\ 00\ 00$ $00\ 00\ 00 \dots 00\ 00\ 00$	$00\ 00\ 00 \dots 00\ 00\ 00$ $00\ 00\ 00 \dots 00\ 00\ 00$
$P_{1,0} P_{1,1} P_{1,2} \dots P_{1,n-1} P_{1,n}$ $P_{3,0} P_{3,1} P_{3,2} \dots P_{3,n-1} P_{3,n}$	$00\ 00\ 00 \dots 00\ 00\ 00$ $00\ 00\ 00 \dots 00\ 00\ 00$
VALID IMAGE EVEN FIELD	HORIZONTAL BLANKING
$P_{m-1,0} P_{m-1,1} \dots P_{m-1,n-1} P_{m-1,n}$ $P_{m+1,0} P_{m+1,1} \dots P_{m+1,n-1} P_{m+1,n}$	$00\ 00\ 00 \dots 00\ 00\ 00$ $00\ 00\ 00 \dots 00\ 00\ 00$
VERTICAL ODD BLANKING	VERTICAL/HORIZONTAL BLANKING
$00\ 00\ 00 \dots 00\ 00\ 00$ $00\ 00\ 00 \dots 00\ 00\ 00$	$00\ 00\ 00 \dots 00\ 00\ 00$ $00\ 00\ 00 \dots 00\ 00\ 00$
$00\ 00\ 00 \dots 00\ 00\ 00$ $00\ 00\ 00 \dots 00\ 00\ 00$	$00\ 00\ 00 \dots 00\ 00\ 00$ $00\ 00\ 00 \dots 00\ 00\ 00$



## Image Flow Processor

The MT9V135 IFP consists of a color processing pipeline, and a measurement and control logic block (the camera controller). The stream of raw data from the sensor enters the pipeline and undergoes several transformations. Image stream processing starts with conditioning the black level and applying a digital gain. The lens shading block compensates for signal loss caused by the lens.

Next, the data is interpolated to recover missing color components for each pixel. The resulting interpolated RGB data passes through the current color correction matrix (CCM), gamma, and saturation corrections, and is formatted for final output.

The measurement and control logic continuously accumulate image brightness and color statistics. Based on these measurements, the IFP calculates updated values for exposure time and sensor analog gains that are sent to the sensor core through the control bus.

### Black Level Conditioning

The sensor core black level calibration works to maintain black pixel values at a constant level, independent of analog gain, reference current, voltage settings, and temperature conditions. If this black level is above zero, it must be reduced before color processing can begin. The black level subtraction block in the IFP re-maps the black level of the sensor to zero prior to lens shading correction. Following lens shading correction, the black level addition block provides capability for another black level adjustment. However, for good contrast, this level should be set to zero.

### Digital Gain

Controlled by auto exposure logic, the input digital gain stage amplifies the raw image in low-light conditions. (Range: x1–x8).

### Test Pattern

A built-in test pattern generator produces a test image stream that can be multiplexed with the gain stage. The test pattern can be selected through register settings.

### Lens Shading Correction

Inexpensive lenses tend to attenuate image intensity near the edges of pixel arrays. Other factors also cause signal and coloration differences across the image. The net result of all these factors is known as lens shading. Lens shading correction (LC) compensates for these differences.

Typically, the profile of lens shading induced anomalies across the frame is different for each color component. Lens shading correction is independently calibrated for the color channels.

### Interpolation and Aperture Correction

A demosaic engine converts the single color per pixel Bayer data from the sensor into RGB (10-bit per color channel). The demosaic algorithm analyzes neighboring pixels to generate a best guess for the missing color components. Edge sharpness is preserved as much as possible.

Aperture correction sharpens the image by an adjustable amount. Sharpening can be programmed to phase out as light levels drop to avoid amplifying noise.



## Defect Correction

This device supports 2D defect correction. In 2D defect detection/correction, pixels with values different from their neighbors by greater than a defined threshold are considered defects unless near the image boundary. The approach is termed 2D, as pixels on neighboring lines as well as neighboring pixels on the same line are considered in both detection and correction.

## Color Correction

To obtain good color rendition and saturation, it is necessary to compensate for the differences between the spectral characteristics of the imager color filter array and the spectral response of the human eye. This compensation, also known as color separation, is achieved through linear transformation of the image with a 3 x 3 element color correction matrix. The optimal values for the color correction coefficients depend on the spectra of the incident illumination and can be programmed by the user.

## Color Saturation Control

Both color saturation and sharpness enhancement can be set by the user, or adjusted automatically by tracking the magnitude of the gains used by the auto exposure algorithm.

## Automatic White Balance

The MT9V135 has a built-in AWB algorithm designed to compensate for the effects of changing scene illumination on the quality of the color rendition. This sophisticated algorithm consists of two major submodules:

- A measurement engine (ME) performing statistical analysis of the image.
- A module selecting the optimal color correction matrix and analog color channel gains in the sensor core.

While the default algorithm settings are adequate in most situations, the user can reprogram base color correction matrices and limit color channel gains. The AWB does not attempt to locate the brightest or grayest elements in the image; it performs in-depth image analysis to differentiate between changes in predominant spectra of illumination and changes in predominant scene colors. Factory defaults are suitable for most applications; however, a wide range of algorithm parameters can be overwritten by the user through the serial interface.

## Auto Exposure

The auto exposure algorithm performs automatic adjustments to image brightness by controlling exposure time and analog gains in the sensor core, as well as digital gain applied to the image. The algorithm relies on the auto exposure measurement engine that tracks speed and amplitude changes in the overall luminance of selected windows in the image.

Back light compensation is achieved by weighting the luminance in the center of the image higher than the luminance on the periphery. Other algorithm features include fast-fluctuating illumination rejection (time averaging), response-speed control, and controlled sensitivity to small changes.

While the default settings are adequate in most situations, the user can program target brightness, measurement window, and other parameters as described above. The auto exposure algorithm enables compensation for a broad range of illumination intensities.



## Electrical Specifications

**Table 5: Electrical Characteristics and Operating Conditions**
 $T_A = 25^\circ\text{C}$ 

Parameter <sup>1</sup>	Condition	Min	Typ	Max	Unit
I/O and core digital voltage (VDD)	N/A	2.5	2.8	3.1	V
LVDS PLL voltage	N/A	2.5	2.8	3.1	V
Video DAC voltage	N/A	2.5	2.8	3.1	V
Analog voltage (VAA)	N/A	2.5	2.8	3.1	V
Pixel supply voltage (VAAPIX)	N/A	2.5	2.8	3.1	V
Leakage current	STANDBY, no clocks			10	$\mu\text{A}$
Imager operating temperature <sup>2</sup>	N/A	-30		+70	$^\circ\text{C}$
Storage temperature	N/A	-30		+125	$^\circ\text{C}$

- Notes:
1. VDD, VAA, and VAAPIX must all be at the same potential to avoid excessive current draw. Care must be taken to avoid excessive noise injection in the analog supplies if all three supplies are tied together.
  2. Customers requiring a similar part with greater temperature range should consider using the Micron MT9V125.

**Table 6: Video DAC Electrical Characteristics**
 $T_A = 25^\circ\text{C}$ ; All table values are estimates until the block is tested and characterized

Parameter	Condition	Min	Typ	Max	Unit
Resolution			10		bits
DNL	Single-ended mode		0.8	1.1	bits
INL	Single-ended mode		5.7	8.1	bits
Output local load	Single-ended mode, output pad (DAC_POS)		75		Ohm
	Single-ended mode, unused output (DAC_NEG)		0		Ohm
Output voltage	Single-ended mode, code 000h		0.02		V
	Single-ended mode, code 3FFh		1.42		V
Output current	Single-ended mode, code 000h		0.6		mA
	Single-ended mode, code 3FFh		37.9		mA
DNL	Differential mode		0.7	1	bits
INL	Differential mode		1.4	3	bits
Output local load	Differential mode per pad (DAC_POS and DAC_NEG)		37.5		Ohm
Output voltage	Differential mode, code 000h, pad dacp		0.37		V
	Differential mode, code 000h, pad dacn		1.07		V
	Differential mode, code 3FFh, pad dacp		1.07		V
	Differential mode, code 3FFh, pad dacn		0.37		V
Output current	Differential mode, code 000h, pad dacp		0.6		mA
	Differential mode, code 000h, pad dacn		37.9		mA
	Differential mode, code 3FFh, pad dacp		37.9		mA
	Differential mode, code 3FFh, pad dacn		0.6		mA
Differential output mid level	Differential mode		0.72		V
Supply current	Estimate			55	mA



## MT9V135: SOC VGA Digital Image Sensor Electrical Specifications

**Table 7: Digital I/O Parameters**

Signal	Parameter	Definition	Condition	Min	Typ	Max	Unit
All Outputs		Load capacitance		1		30	pF
		Output signal slew	2.8V, 30pF load		0.72		V/ns
		Output signal slew	2.8V, 5pF load		1.25		V/ns
	V <sub>OH</sub>	Output high voltage		2.5	2.8	3.1	V
	V <sub>OL</sub>	Output low voltage		-0.3		0.3	V
	I <sub>OH</sub>	Output high current	V <sub>DD</sub> = 2.8V, V <sub>OH</sub> = 2.4V	16		26.5	mA
I <sub>OL</sub>	Output low current	V <sub>DD</sub> = 2.8V, V <sub>OL</sub> = 0.4V	15.9		21.3	mA	
All Inputs	V <sub>IH</sub>	Input high voltage	V <sub>DD</sub> = 2.8V	1.48			V
	V <sub>IL</sub>	Input low voltage	V <sub>DD</sub> = 2.8V			1.43	V
	I <sub>IN</sub>	Input leakage current		-2		2	μA
	Signal CAP	Input signal capacitance			3.5		pF
EXTCLK	freq	Master clock frequency	Absolute minimum	2			MHz
			VGA at 30 fps		27		MHz

## Power Consumption

**Table 8: Power Consumption**

T<sub>A</sub> = Ambient = 25°C; All supplies at 2.8V

Mode	Sensor (mW)	Image-Flow Proc (mW)	I/Os (mW) <sup>1</sup>	DAC (mW)	LVDS (mW)	Total (mW)
Active mode <sup>2</sup>	60	100	10	150	80	400
Standby						0.56

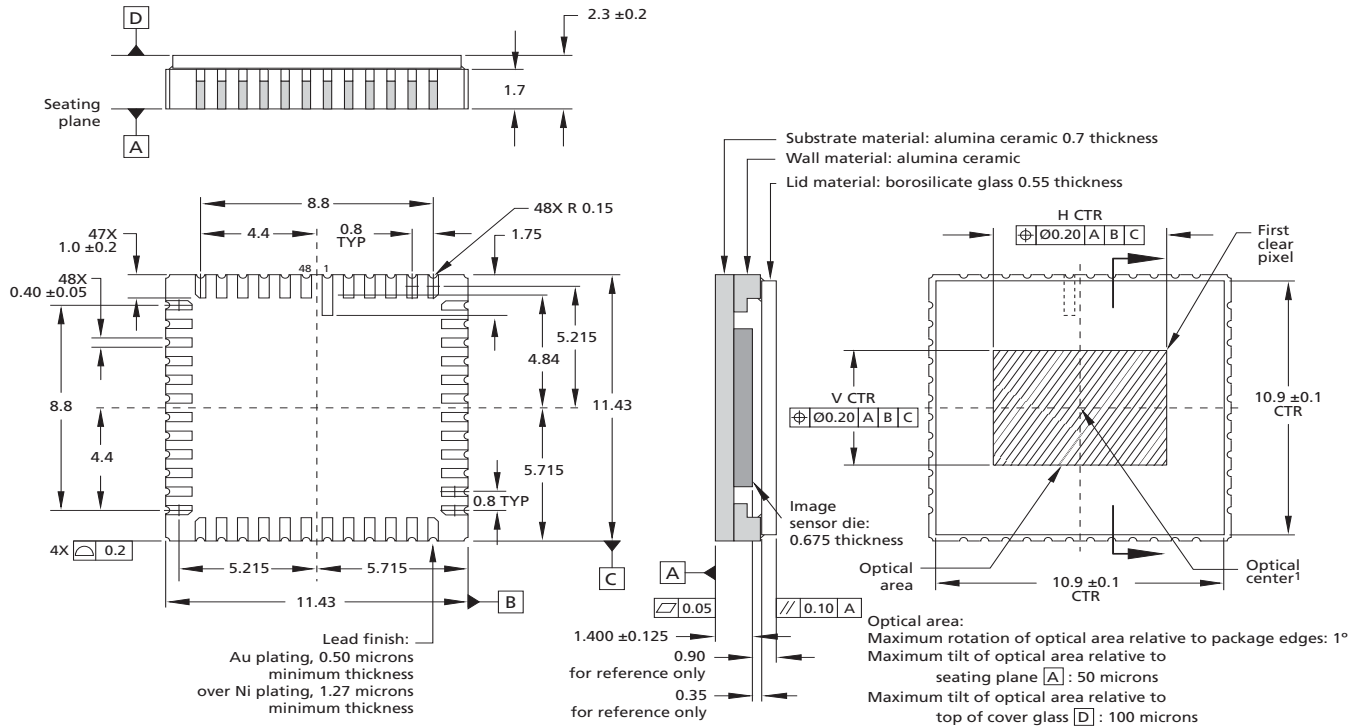
- Notes: 1. 10pF nominal.  
2. (NTSC or PAL) and LVDS should not be operated at the same time.



# MT9V135: SOC VGA Digital Image Sensor Package Diagram

## Package Diagram

**Figure 10: 48-Pin CLCC Package Outline Drawing**



- Notes: 1. Optical center = package center.
- 2. All dimensions are in millimeters.



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**Preliminary: This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.**





## Revision History

Rev. B .....	3/28/2007
<ul style="list-style-type: none"><li>• Updated package drawing.</li></ul>	